Innovative Use of DSP Technology in Space: FORTE Event Classifier

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Abstract--The Fast On-Orbit Recording of Transient Events (FORTE) small satellite will field a digital signal processor (DSP) experiment for the purpose of classifying radio-frequency (rf) transient signals propagating through the earth's ionosphere. Designated the Event Classifier experiment, this DSP experiment uses a single Texas Instruments' SMJ320C30 DSP to execute preprocessing, feature extraction, and classification algorithms on down-converted, digitized, and buffered rf transient signals in the frequency range of 30 to 300 MHz. A radiation-hardened microcontroller monitors DSP-abnormalities and supervises spacecraft command communications. On-orbit evaluation of multiple algorithms is supported by the Event Classifier architecture. Ground-based commands determine the subset and sequence of algorithms executed to classify a captured time series. Conventional neural network classification algorithms will be some of the classification techniques implemented on-board FORTE while in a low-earth orbit. Results of all experiments, after being stored in DSP flash memory, will be transmitted through the spacecraft to ground stations. The Event Classifier is a versatile and fault-tolerant experiment that is an important new space-based application of DSP technology.

I. Introduction

FORTE (Fast On-Orbit Recording of Transient Events) is a United States of America Department of Energy small-satellite experiment scheduled for launch in mid-1995. A 10-meter pseudo-log-periodic boom antenna coupled to state-of-the-art analog and analog-to-digital electronics will capture VHF (30-300 MHz) electromagnetic transients. From the space-based vantage point, the main sources of natural electromagnetic transients are expected to be lightning signals[1]. Changes in the ionospheric total electron content (TEC) will produce variations in the wideband frequency-dispersion profile of the transient signals produced below the ionosphere. The transient signals will be obscured not only by background noise, but also by man-made clutter (e.g., continuous-wave carriers, burst communications, chirped-radar signals, etc.).

To study the reduction of telemetry signals to the ground, FORTE utilizes an advanced signal analyzer called the Event Classifier (EC). The EC incorporates a single Texas Instruments' SMJ320C30 DSP, which will execute neural network-based classification schemes. Communicating only with the Flight Payload Controller (FPC), the EC will receive raw data and return analysis reports via a 16-bit parallel port, and receive commands/code uplinks and return state of health reports via a serial port. Figure 1 shows a partial block diagram of the interconnections between various subsystems of FORTE. The interconnections show that the Event Classifier is a general purpose DSP-based computation system.

II. EC Hardware Design

A. General Implementation

Radiation tolerance is a primary consideration in the design of space-based hardware. With this consideration taken into account, two processor elements are used in the design of the EC. A radiation hardened version of an 80C31 (SA3865) serves as the microcontroller for the EC. A C30 DSP (SMJ320C30), which is less radiation tolerant than the microcontroller, performs all data analysis tasks. By using the microcontroller to monitor the operation of the DSP and perform command/housekeeping communications with the FPC, a more robust system interface is achieved at

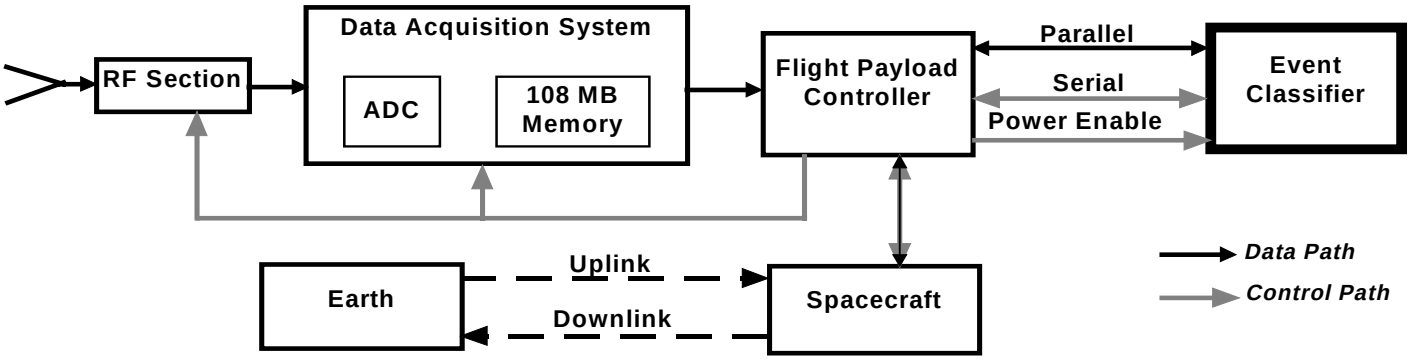

Figure 1 Partial block diagram of subsystem interconnections for the Forte small satellite

the expensive of weight, power usage, and cost, as opposed to using the DSP alone. Figure 2 shows a functional schematic of the Event Classifier.

Memory available to the 8-bit microcontroller consists of 8 Kbytes of radiation-hardened PROM and radiation-hardened SRAM. There is no shared memory between the microcontroller and the DSP. Communication between the microcontroller and the DSP is conducted through an Actel 1280 Field Programmable Gate Array (FPGA) via registers and interrupts. Interrupts are provided to both the microcontroller and DSP when data is available to be read. Memory-address decoding for the microcontroller is performed in the FPGA. Communication between the FPC and the microcontroller is conducted using one of the serial ports of the microcontroller at 9600 baud.

DSP memory accesses and communications are

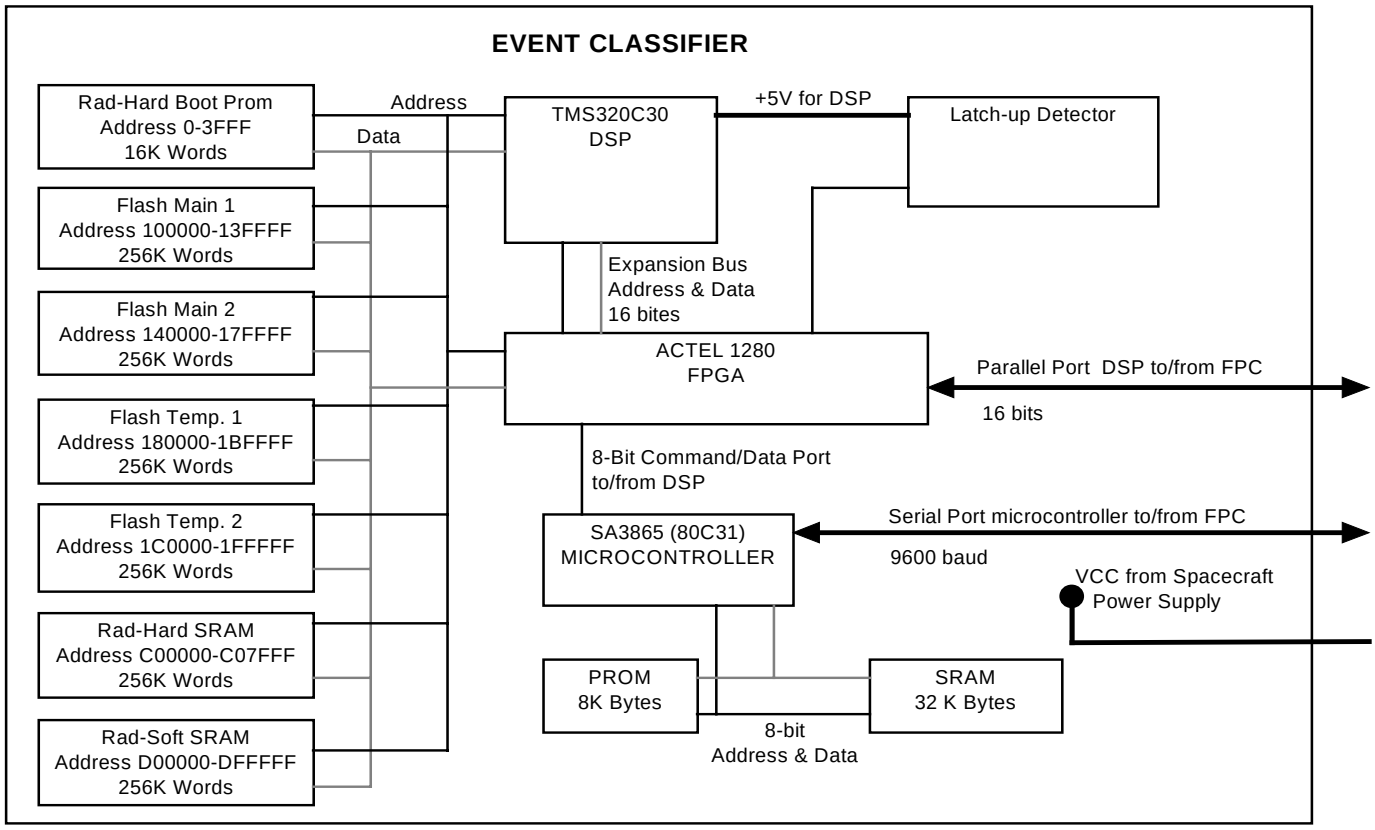

Figure 2 Functional schematic of FORTE Event Classifier.

conducted using the two-bus architecture of the C30 DSP, which allows 32-bit accesses to physical memory over the primary bus and 16-bit accesses to the FPGA over the expansion bus. Primary-bus memory varieties include PROM, SRAM, and Flash memory. The 16 Kwords of rad-hard PROM memory contain boot and upset-recovery firmware. SRAM memory includes 32-Kwords of radiation-hardened memory and 1 Mword of radiation-susceptible memory. The Flash memory is used for data-analysis code execution and for analysis report storage before transmission to the ground. Address decoding for the DSP primary bus is performed by the FPGA.

The FPGA interfaces with both address and 16-bit data to the DSP expansion bus. Data from the expansion bus is forced to 16 bits by using only the lower half of a 32-bit word. Communications with the microcontroller and FPC are conducted over the expansion bus and then through the FPGA via registers. A 16-bit bi-directional parallel port to the FPC is used to input data to the DSP and output analysis reports to the FPC. Since the DSP operating with a 25-MHz clock is significantly faster than the FPC, the only handshaking performed on the parallel port is to interrupt the DSP that the FPC has either written or read data. This handshaking protocol provides the least burden to the FPC, which must contend with demands from the other payload subsystems.

B. Additional Radiation Design Issues

A 5-K rads (Si) total-dose radiation-exposure specification has been determined for the FORTE mission[2]. Previous radiation testing of TMS320C30 DSPs[3], both commercial and military grades, revealed processor failure between 4- and 5-K rads (Si) total-dose exposure. The EC uses the military-grade 1-micron version of the TMS320C30, SMJ320C30, at a slower clock rate than the testing, which may degrade radiation hardness. In order to minimize the burden to the FPC, a mission-defined radiation-hard microcontroller was incorporated into the EC design to monitor the DSP.

Using the expansion bus, the DSP is required to "ping," at least once a second, a watchdog timer circuit in the FPGA. The "ping" operation consists of writing to a specific memory location and subsequently resetting the watchdog counter. If the watchdog times-out, the microcontroller is interrupted and then attempts to communicate with the DSP. Failure of communication forces the microcontroller to reset the DSP and reinitialize data-analysis operations. The watchdog timer can deal effectively with non-destructive latchup of the DSP.

However, the DSP is also susceptible to destructive latchup failure. The microcontroller would not be able to respond fast enough should destructive latchup occur. To prevent a destructive latchup failure from progressing to the destruction of the DSP, a current-monitoring latchup-protection circuit, shown in Figure 3, supports the DSP. The latchup-protection circuit autonomously disconnects power from the DSP and interrupts the microcontroller should the current level exceed threshold. Some adjustment of the current-level threshold is provided to the microcontroller. This inventive circuit prevents catastrophic events from terminating the Event Classifier experiment.

Some on-orbit device testing of the DSP is contemplated provided mission related issues do not overshadow the testing. Testing would involve the exercising of DSP internal memory, which is not used in normal operations, for the detection of bit upsets. The DSP also contains two serial ports and two timers that may be interconnected for testing of their operations in orbital conditions. Other testing is presently undetermined.

In addition to the DSP being susceptible to radiation, the 1-Mword block of SRAM that supports the DSP is also susceptible to bit upsets. To combat this bit upset problem, error control coding will be implemented on access to the memory. Extended double-error-correcting codes will be implemented for codewords of length 128-bits and possibly 512-bits. Both codes will be block codes of some implementation.

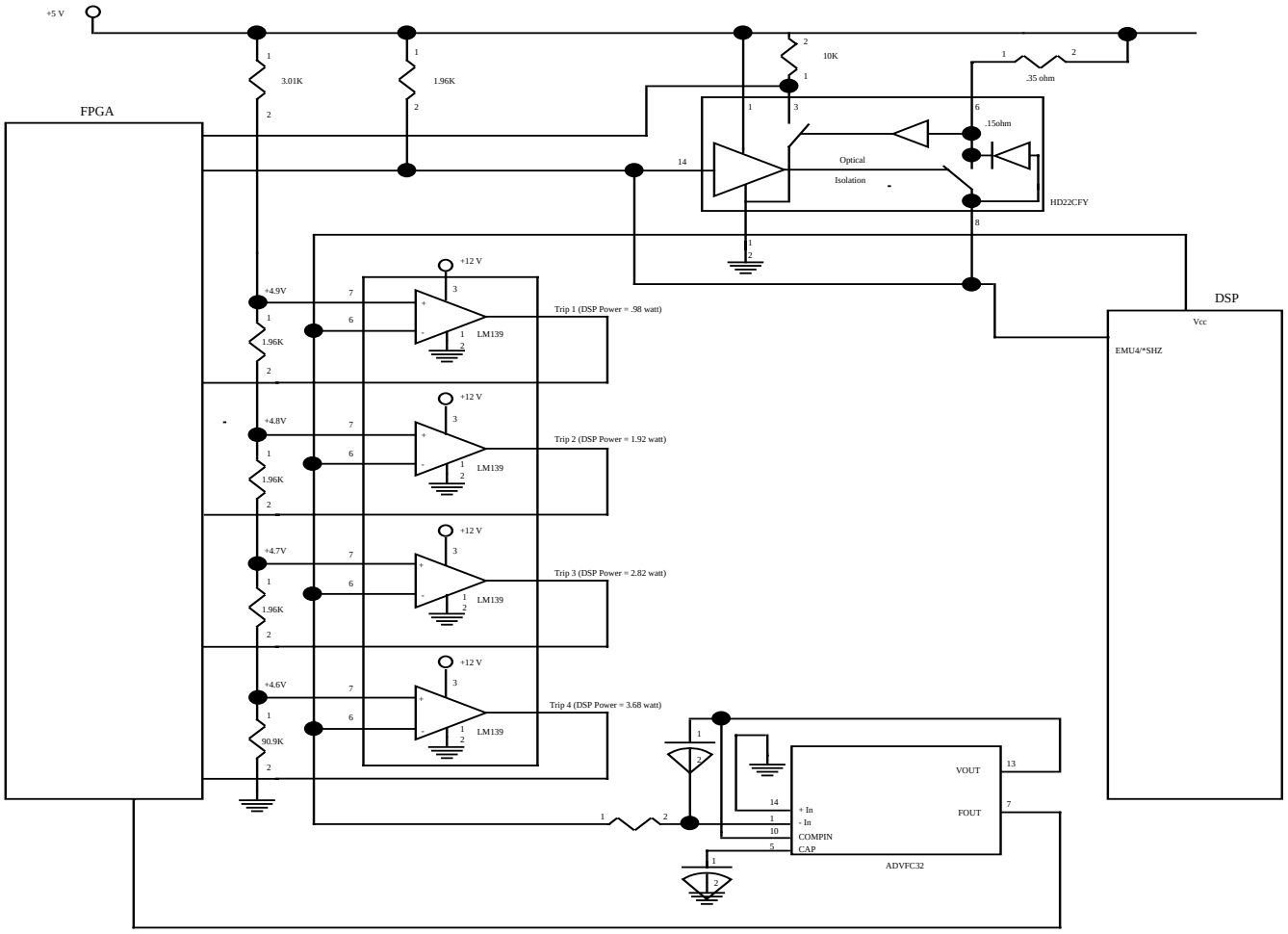

Figure 3 Latch-Up Detector circuit.

C. Emulator-Port Buffering

The DSP incorporates an extremely useful emulator port for software development and hardware debugging. However, upon using this XDS510 PC-based emulator with prototype hardware, the need for tri-state buffering became apparent. The flight Actel FPGA is a one-time programmable device, so a Xilinx FPGA was used for development. This prototype FPGA configured unreliably with the emulator connected. This problem was traced to a 0.8 Vdc voltage that was observed on the dormant prototype target system, due to a stray voltage that originated from the emulator. To solve this problem, a tri-state buffer was placed on the emulator port. The stray voltage would have been unacceptable when working with flight hardware. The emulator-buffer circuit is shown in Figure 4.

III. EC Software Design

The EC relies on the microcontroller to intercept all commands from the FPC. Operating on bytes, the microcontroller parses out commands, which are provided over the serial link, and places them in FPGA registers. The same procedure occurs when recently developed classification-algorithm codes and algorithm sequences, intended for execution on the DSP, are uplinked to the EC. Housekeeping and state-of-heath information are collected and formatted by the microcontroller for once-a-second transmission over the serial link to the FPC. Also the microcontroller formats requests from the DSP

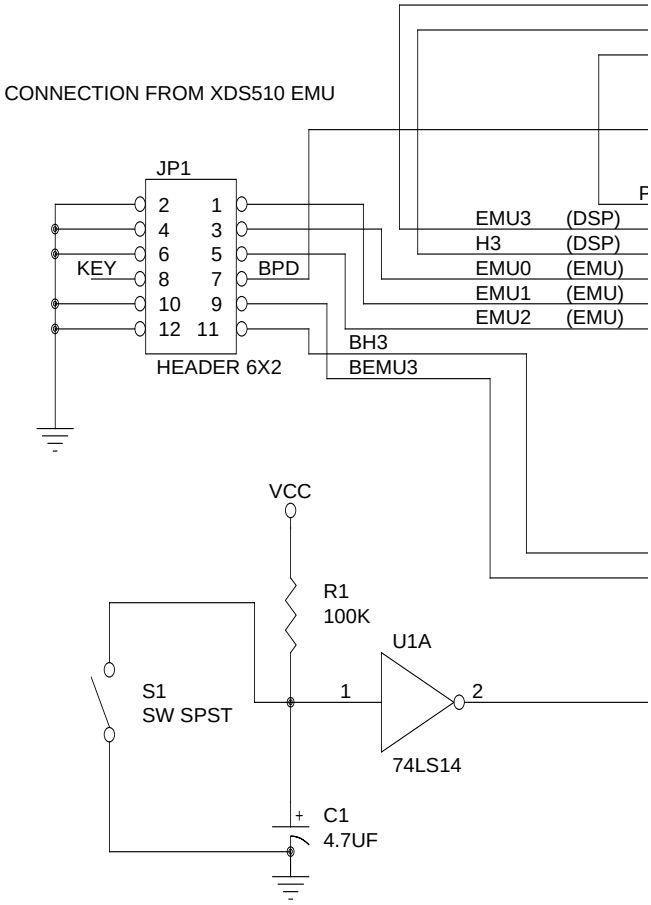

Figure 4. Emulator buffer circuit.

to the FPC. While the microcontroller is conducting communications tasks, it continuously monitors the DSP for latchup occurrence.

The DSP is held in reset until the microcontroller releases it. Once released, the DSP executes boot and test operations. Instructions from the ground, transmitted through the microcontroller, command the DSP to upload new code/algorithm sequences, execute algorithms, or download computational or memory-test results.

Executable code for the algorithms is held in Flash memory along with values of pre-defined variables. A function table is used to reference individual algorithms. Thus a sequence of algorithms can be assembled from the function table to operate on the data. The results of the computations are placed in Flash memory for downloading to a ground station at some later time.

The time-series data provided to the EC can be in two different formats. One format consists of a sample rate of 300 Msps, a baseband bandwidth of 90 MHz, and 8 bits of quantization. The other format consist of a sample rate of 50 Msps, a baseband bandwidth of 20 MHz, and 12 bits of quantization. Both formats are mixed down to their relative baseband bandwidth from the frequency range of 10 to 320 MHz. The duration of the time-series records can be extremely large (e.g., several milliseconds). However, the EC is constrained to time-series lengths of 256k samples or less.

The conventional pattern-classification paradigm consists of the following functional blocks: (1) Preprocessing and Enhancement, (2) Interest-Point Location, (3) Feature Extraction, (4) Classification, and (5) Parameter Estimation, which is shown in Figure 5. Even with such a paradigm, no general methodology exists for selecting and implementing specific pattern-classification techniques. Each application of pattern classification requires an application-driven solution. As knowledge is gained through greater exposure to real-world data, the algorithms for each of the functional blocks can be redeveloped and improved.

The current baseline algorithm sequence consists of: a sub-band trigger for interests-point location; a spectrogram generator for feature extraction; and a neural-network self-organizing map for classification. Preprocessing is not implemented in

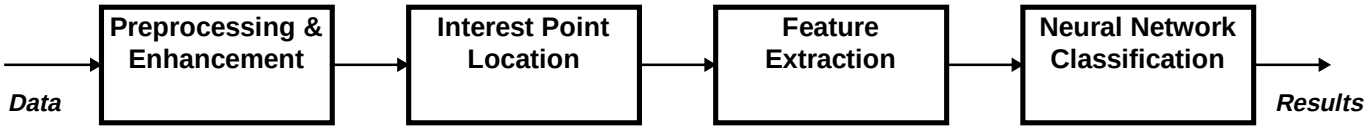

Figure 5 Pattern-Classification paradigm.

the baseline algorithm sequence. However, a unique device, known as the Adaptive Pre-whitener, will be place at the rf front-end to reduce carrier signals. The software sub-band trigger is necessary for interest-point location because the acquisition system may false trigger.

The spectrogram generator provides a time-frequency representation of the signal. This type of representation provides a very clear interpretation of the frequency-dispersive nature of the ionosphere, which is conveyed in the signal. Performed properly[4], the short-time Fourier transforms yields a spectrogram that provides an accurate representation of the instantaneous frequency. The frequency-dispersive nature of the ionosphere yields approximately a concaved-upward quadratic instantaneous-frequency representation of impulsive terrestrial sources[5]. The spectrogram values are used as features for classification.

The neural network uses the spectrogram magnitude values as the input feature vector. The instantaneous-frequency profile will vary depending on the ionospheric conditions. By using a self-organizing map[6], the weights of an unspecified neuron are allowed to "learn" and converge to an exemplar representation of the ionospheric frequency dispersion. After an appropriate training period, the weights of the neural network, which will be downloaded, are fixed and subsequent winning neurons provide classification of the signal. Analysis of actual data show that different neurons respond to noise only, clutter, or desired signals.

Other algorithms to be tried include: adaptive line suppression for preprocessing; wavelet representations for feature extraction and interest-point location; model-based neural networks for feature extraction; and other forms of neural networks for classification. The ability to uplink new algorithms provides a space-base platform for the evaluation of different classification realizations. The Event Classifier is a versatile pattern classification test bed that is an innovative uses of DSP technology in space.

IV. Summary

The Event Classifier experiment on the FORTE small satellite will provide DSP technology the opportunity to expand its role in space-based applications. Having the capability to program the DSP from the ground allows for a versatile test bed to evaluate pattern classification techniques and radiation-hardness issues.

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